What is claimed is:

1. A transistor circuit comprising:

an input node

an output node;

an array of heterojunction bipolar transistor (HBT) unit cells, each HBT unit cell comprising an HBT including a collector coupled to the output node, including a horseshoe-shaped emitter coupled to a ground node, and including a strip-shaped base coupled to the input node.

2. An amplifier comprising:

a chip including:

a plurality of transistor arrays, each transistor array comprising a plurality of transistors, each transistor including a collector coupled to an output node, including a base coupled to an input node, and including an emitter coupled to a ground node, and

a plurality of local pads, each local pad being disposed adjacent to a corresponding group of ones of said plurality of transistor arrays and coupled to the output nodes of said corresponding group of transistor arrays; and

a global pad outside the chip coupled to each of the plurality of local pads by wirebonds.

3. A reference current generator comprising:

a first bipolar junction transistor including a collector, including an emitter, and including a base coupled to a voltage mode node;

a first resistor including a first terminal coupled to the emitter of the first bipolar junction transistor and including a second terminal coupled to a ground node;

a second bipolar junction transistor including a collector, including an emitter coupled to the ground node, and including a base;

a second resistor including first and second terminals coupled to the collector of the first and second bipolar junction transistors, respectively;

a third resistor including a first terminal coupled to a reference voltage node and including a second terminal coupled to the collector of the second bipolar junction transistor;

a third bipolar junction transistor including a collector coupled to a supply voltage node, including an emitter coupled to the base of the second bipolar junction transistor, and including a base coupled to the collector of the second bipolar junction transistor; and

a fourth resistor including a first terminal coupled to the emitter of the third bipolar junction transistor and including a second terminal coupled to the ground node.